

APPLICATION NO. 10/730855

May 17, 2005

YR

CLMPTO

1. (Currently Amended) A ferroelectric random access memory (FeRAM) capacitor, comprising:

an active matrix including a semiconductor substrate, field oxide regions, a source/drain region, a first interlayer dielectric (ILD) and a storage node contact;

a capacitor stack including a bottom electrode, a ferroelectric layer and a top electrode, wherein the bottom electrode, the ferroelectric layer and the top electrode are formed on the active matrix and a width of the capacitor stack is relatively larger than that of the storage node;

a second ILD enclosing capacitor stack, wherein the top face of the top electrode is not covered with the second ILD and the top face of the top electrode is lower than the top face of the second ILD; and

a plate line formed on the top face of the top electrode and predetermined portions of the second ILD, the width of the plate line being larger than that of the top electrode.

2. (Original) The FeRAM capacitor as recited in claim 1, further comprising:

a first glue layer formed between the first ILD and the bottom electrode; and

a second glue layer formed between the second ILD and the plate line.

3. (Original) The FeRAM capacitor as recited in claim 2, wherein the first glue layer and the second glue layer employ alumina ( $\text{Al}_2\text{O}_3$ ).

4. (Original) The FeRAM capacitor as recited in claim 3, wherein the first glue layer and the second glue layer are formed by using a method selected from the group consisting of an atomic layer deposition (ALD), a chemical mechanical polishing (CMP) and a physical vapor deposition (PVD).

5. (Original) The FeRAM capacitor as recited in claim 4, wherein the first glue layer and the second glue layer have the thickness in the range of about 5 Å to about 50 Å.

6. (Cancelled)

7. (Original) The FeRAM capacitor as recited in claim 1, wherein the second ILD uses a material selected from the group consisting of phosphorous silicate glass (PSG), spin-on-glass (SOG), undoped silicate glass (USG) and tetra-ethyl-ortho-silicate (TEOS).

8. (Original) The FeRAM capacitor as recited in claim 7, wherein the second ILD is a double layer in which a first layer is formed on the first ILD and sidewalls of the capacitor stack for preventing oxygen diffusion and a second layer is formed on the first layer.

9. (Original) The FeRAM capacitor as recited in claim 8, wherein the first layer uses a material selected from the group consisting of titanium oxide (TiO<sub>2</sub>), TEOS and Al<sub>2</sub>O<sub>3</sub>.

10. (Original) The FeRAM capacitor as recited in claim 8, wherein the second layer uses a material selected from the group consisting of PSG, SOG, USG and TEOS.

11. (Original) The FeRAM capacitor as recited in claim 1, wherein the bottom electrode is formed by using a method selected from the group consisting of the CVD, the PVD, the ALD and a plasma enhanced ALD (PEALD).

12. (Original) The FeRAM capacitor as recited in claim 11, wherein the bottom electrode employs a material selected from the group consisting of platinum (Pt), iridium (Ir), ruthenium (Ru), rhenium (Re), rhodium (Rh) and a combination thereof.

13. (Original) The FeRAM capacitor as recited in claim 1, wherein the ferroelectric layer is formed with the thickness in the range of about 50 Å to about 2,000 Å by using a method selected from the group consisting of a spin-on coating, the PVD, the CVD and the ALD.

14. (Original) The FeRAM capacitor as recited in claim 13, wherein the ferroelectric layer uses a material selected from the group consisting of bismuth lanthanum titanate (BLT), strontium bismuth tantalate (SBT), strontium bismuth niobate tantalate (SBTN) and lead zirconate titanate (PZT).

15. (Original) The FeRAM capacitor as recited in claim 1, wherein the top electrode is formed with the thickness in the range of about 100 Å to about 1,000 Å by using a method selected from the group consisting of the CVD, the PVD, the ALD and the PEALD.

16. (Original) The FeRAM capacitor as recited in claim 15, wherein the top electrode uses a material selected from the group consisting of Pt, Ir, Ru, IrO<sub>2</sub>, RuO<sub>2</sub>, Pt/IrO<sub>2</sub>, Pt/IrO<sub>2</sub>/Ir, IrO<sub>2</sub>/Ir, RuO<sub>2</sub>/Ru, Pt/RuO<sub>2</sub>/Ru and Pt/RuO<sub>2</sub>.

17. (Original) The FeRAM capacitor as recited in claim 1, wherein the plate line is formed with the thickness in the range of about 500 Å to about 3,000 Å by using a method selected from the group consisting of the PVD, the CVD and the ALD.

CLAIMS 18-49 (CANCELLED)